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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,063	11/13/2001	Miaochen Wu	3070.1008-000	2756

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EXAMINER	
SAMS, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,063	WU ET AL.	
	Examiner	Art Unit	
	Matthew C. Sams	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed February 9, 2004 has been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 9, 11 and 16 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Matthews (US-4,713,630).

Regarding claim 1, Matthews teaches a circuit that has a locking detection and a frequency acquisition apparatus along with a phase lock loop. (Col. 1 lines 7-10) Matthews teaches a comparator connected to a locking indicator signal in the phase lock loop, where the voltage level of the locking indicator signal determines the open/closed state of a switch. (Col. 2 line 64 through Col. 3 line 22) Matthews teaches of a sweeping signal generator that pushes the phase lock loop inside a locking range. (Col. 1 lines 64-68)

Regarding claim 9, Matthews teaches a comparator that is continually searching for lock-in status outputs a voltage, which controls a switch in the phase lock loop. (Col.

2 line 64 through line 22) Matthews' comparator inherently sends a plurality of pulses in order to continually search.

Regarding claim 11, Matthews teaches a three-terminal switch coupled to a comparator. (Col. 2 lines 64 through line 22 and Fig. 2 [24])

Regarding claim 16, the limitations of claim 16 are rejected as the same reason set forth in claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-8, 10, 12-13, 17-22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews and Black (US-5,751,195).

Regarding claim 2, Matthews teaches the limitations of claim 1. Matthews differs from the claimed invention in not specifically stating the sweeping signal is periodic. However, Black teaches a sweeping output from an oscillator that is periodic. (Col. 3 lines 7-11) At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate a periodic sweeping signal of Black with a receiver having locking detection and frequency acquisition like that of Matthews. One of ordinary skill in the art would have been motivated to do this since having a versatile

periodic sweeping signal allows for a wider range of input frequencies. (Col. 1 lines 38-42)

Regarding claim 3, Black teaches a frequency of the periodic sweeping signal that is lower than the frequency of a receive signal in the phase lock loop. (Col. 1 lines 57-62)

Regarding claim 4, Black teaches a sweeping periodic signal that is a triangular waveform. (Col. 3 lines 7-11 and 59-63)

Regarding claim 5, Black teaches a sweeping periodic signal that is a square waveform. (Col. 3 lines 7-11)

Regarding claim 6, Black teaches a sweeping periodic signal that is a sinusoidal waveform. (Col. 3 lines 7-11)

Regarding claim 7, Black teaches a frequency of the periodic sweeping signal that is at least an order of magnitude lower than the frequency of received frames on the received signal. (Col. 1 lines 57-62)

Regarding claim 8, Black teaches a period of the periodic sweeping signal of 1200 milliseconds and the period of the received signal is 10 microseconds. The period of a signal is the inverse of the frequency. (Col. 1 lines 57-62)

Regarding claim 10, Matthews teaches a locking indicator that is an output of a differential amplifier in a phase lock loop. (Col. 2 lines 64-68 and Col. 3 lines 1-7) Black teaches an integrator circuit coupled to a logic switch in a phase lock loop. (Col. 4 lines 31-60)

Regarding claim 12, Black teaches an integrator circuit coupled to a logic switch in a phase lock loop. (Col. 4 lines 31-60)

Regarding claim 13, Black teaches a switch coupled to the inverting input of a comparator followed by a not gate, in the integrator of the phase lock loop. (Fig. 2 [21])

Regarding claim 17, the limitations of claim 17 are rejected as the same reason set forth in claim 2.

Regarding claim 18, the limitations of claim 18 are rejected as the same reason set forth in claim 3.

Regarding claim 19, the limitations of claim 19 are rejected as the same reason set forth in claim 4.

Regarding claim 20, the limitations of claim 20 are rejected as the same reason set forth in claim 5.

Regarding claim 21, the limitations of claim 21 are rejected as the same reason set forth in claim 6.

Regarding claim 22, the limitations of claim 22 are rejected as the same reason set forth in claim 7.

Regarding claim 23, the limitations of claim 23 are rejected as the same reason set forth in claim 8.

Regarding claim 24, Matthews teaches a plurality of pulses is generated until the phase lock loop is within the locking range. (Col. 1 lines 66-68) Black teaches a plurality of received frames. (Col. 1 lines 57-62)

6. Claims 14, 25, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews and Takla (US-6,295,327).

Regarding claim 14, Matthews teaches the limitations of claim 1. Matthews differs from the claimed invention in failing to state a comparator that creates a pulse during the switch close signal while the apparatus is in a frame synchronization period of a received frame and the voltage level of the locking indicator signal is outside the locking range of the phase lock loop. However, Takla teaches a phase locked loop with reduced synchronization time by locking onto a training mode clock signal while the data signal is outside the locking range. (Col. 3 lines 51-65) At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the reduced synchronization time of Takla with the receiver with locking detection and frequency acquisition of Matthews. One of ordinary skill in the art would have been motivated to do this since the phase lock loop is able to save time and become locked onto the signal faster than normal. (Col. 3 lines 4-13)

Regarding claim 25, the limitations of claim 25 are rejected as the same reason set forth in claim 14.

Regarding claim 27, Matthews teaches a circuit that has a locking detection and a frequency acquisition apparatus along with a phase lock loop. (Col. 1 lines 7-10) Matthews teaches a comparator connected to a locking indicator signal in the phase lock loop, where the voltage level of the locking indicator signal determines the open/closed state of a switch. (Col. 2 lines 64-68 and Col. 3 lines 1-7) Matthews teaches of a sweeping signal generator that pushes the phase lock loop inside a locking

range. (Col. 1 lines 64-68) Matthews' local oscillator is a voltage-controlled oscillator. (Fig. 2 [14]) One of ordinary skill in the art knows a voltage-controlled oscillator's frequency output is controlled by the voltage input. Takla teaches a phase locked loop with reduced synchronization time by locking onto a training mode clock signal while the data signal is outside the locking range. (Col. 3 lines 51-65)

Regarding claim 28, the limitations of claim 28 are rejected as the same reason set forth in claim 27.

Claims 15 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews and Takla as applied to claim 14 above, and further in view of Stribling et al. (US-5,144,260 hereinafter, Stribling).

Regarding claim 15, Matthews and Takla teach the limitations of claim 14. Matthews and Takla differ from the claimed invention in failing to mention that the common mode voltage level is 2.5 volts and the voltage level in the range 2.4-2.6 volts on the locking indicator signal is within the locking range. However, Stribling teaches a voltage of 2.5 volts that is used for locking and as a reference value for pull/push the signal level. (Col. 4 lines 49-68) At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate a reference value for pull/push the signal levels with the receiver with locking detection and frequency acquisition of Matthews and Takla. One of ordinary skill in the art would have been motivated to do this since having a mid point value for the range of values helps to eliminate the effects of the perturbations. (Col. 4 lines 49-68)

Regarding claim 26, the limitations of claim 26 are rejected as the same reason set forth in claim 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Sams whose telephone number is (703)305-0810. The examiner can normally be reached on M-F 7:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis Kuntz can be reached on (703)305-4708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MCS
12/9/2004

GEORGE ENG
PRIMARY EXAMINER